

Claims

[c1] What is claimed is:

1. A method of fabricating an interconnect structure having reduced internal stress, comprising the steps of:
providing a semiconductor substrate having a base dielectric layer thereon;
forming a damascened interconnect structure in the base dielectric layer;
capping the damascened interconnect structure and the base dielectric layer with a first dielectric barrier;
executing a first chemical vapor deposition (CVD) process within a CVD reactor to deposit a first low-k dielectric film having a pre-selected thickness onto the first dielectric barrier;
executing a first cooling process within the CVD reactor for cooling down the first low-k dielectric film;
executing a second CVD process within the CVD reactor to deposit a second low-k dielectric film having the pre-selected thickness onto the first low-k dielectric film;
executing a second cooling process within the CVD reactor for cooling down the first and second low-k dielectric films, wherein the first and second low-k dielectric films constitute a low-k film stack having reduced internal

stress; and

capping the low-k film stack with a second dielectric barrier.

[c2] 2.The method according to claim 1 wherein the first and second low-k dielectric films have substantially the same compositions.

[c3] 3.The method according to claim 1 wherein the pre-selected thickness is about 0.1~0.15 microns.

[c4] 4.The method according to claim 1 wherein the first dielectric barrier comprises silicon nitride.

[c5] 5.The method according to claim 1 wherein the second dielectric barrier comprises silicon nitride.

[c6] 6.The method according to claim 1 wherein both of the first and second low-k dielectric films have a dielectric constant that is less than 3.0.

[c7] 7.The method according to claim 1 wherein the damascened interconnect structure comprises a barrier layer and a copper core that are embedded in the base dielectric layer.

[c8] 8.A copper damascene process, comprising:
providing a semiconductor substrate having a base dielectric layer thereon;

forming a first damascened copper interconnect structure in the base dielectric layer;
capping the first damascened copper interconnect structure and the base dielectric layer with a dielectric barrier;
executing multiple chemical vapor deposition (CVD) cycles within a CVD reactor to deposit a low-k dielectric film stack on the first dielectric barrier until thickness of the low-k dielectric film stack reaches a desired value, wherein each of the CVD cycles comprises: (1) chemical vapor depositing a low-k dielectric film having a pre-selected thickness; and (2) cooling down the low-k dielectric film within the CVD reactor; and
forming a second damascened copper interconnect structure in the low-k dielectric film stack, wherein the first damascened copper interconnect is electrically connected to the second damascened copper interconnect structure.

- [c9] 9.The method according to claim 8 wherein the pre-selected thickness is about 0.1~0.15 microns.
- [c10] 10.The method according to claim 8 wherein the dielectric barrier comprises silicon nitride.
- [c11] 11.The method according to claim 8 wherein the low-k dielectric film stack has a dielectric constant that is less than 3.0.

[c12] 12. The method according to claim 8 wherein the damascened copper interconnect structure comprises a barrier layer and a copper core that are embedded in the base dielectric layer.